Hall Ticket Number:

Code No. : 16450 H

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (Honours) VI-Semester Main Examinations, May/June-2023

FPGA based System Design

(E.C.E.)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	What are the different types of FPGA, based on programming type?	2	1	1	1	1
2.	Mention three main functions of an I/O pad in an FPGA..	2	1	1	1	1
3.	What is the range of decimal numbers in 2's complement numbering system for a binary number with M integer bits?	2	1	2	1	1
4.	How many logical functions can be formed with 3 variables? Explain.	2	1	2	1	1
5.	Find the minimum number of bits required for storing the result of the arithmetic operation (A + B*C), where A is an 8-bit number and B, C are each 6-bit numbers.	2	3	3	2	1
6.	How can an XOR function act as parity generator?	2	1	3	1	1
7.	Identify the minimum number of D Flip Flops required in a counter with an input frequency of $5x10^5$ Hz and an output frequency of 100Hz.	2	2	4	2	1
8.	Write the differences between Moore and Mealy type of State Machine.	2	1	4	1	1
9.	How many parts of 1K x 4 SRAMs will be needed to construct a 16K x 16 SRAM?	2	2	5	1	1
10.	Assuming 1 pin for chip-select, and 1 pin for rd/wr, how many total signal pins will be present on the above 1K x 4 SRAM?	2	2	5	1	1
	Part-B (5×8 = 40 Marks)					
11. a)	Explain FPGA architecture with a neat block diagram.	4	2	1	1	1
b)	Draw the Flow Diagram for Programming an FPGA using Xilinx Vivado Tools. What is the role of a constraint file?	4	2	1	1	1
12. a)	Differentiate between Blocking and Non-Blocking assignments with suitable examples of where each type of assignment is used.	4	4	2	1	1
b)	Implement the function $F = \sum (1,4,7,8,10,15,18,21,25,28,31)$ using a 5-variable LUT, constructed from 4-variable LUTs.	4	4	2	3	1

Contd... 2

13. a)	An 8-to-3 priority encoder has data inputs in increasing order of priority as follows: A, B, C, D, E, F, G, H. It has also got a single bit output V which is 1 if any one or more bits are asserted. Derive the simplified logic equations for the priority outputs P2, P1, P0 and also for the output V.	4	3	3	3	1
b)	Design full adder using **only** 2x1 multiplexers.	4	4	3	3	1
14. a)	Describe the conversion procedure for converting a T-Flip flop into a JK- flip flop. Draw the circuit diagram.	4	4	4	2	1
b)	Draw a **Moore** State diagram to show the detection of the bit-sequence **11001**. Overlapping sequences must be detected. Write the output of the state machine when the 20-bit input sequence is **1100_0010_0110_0110_0011.**	4	3	4	2	1
15. a)	Design an SRAM of 16Kx8 using 4Kx8 SRAMs such that addresses 0-3 are in the first SRAM, addresses 4-7 are in the next SRAM and so on...	4	4	5	1	1
b)	Compare and Contrast the Verilog code written for a Testbench versus the Verilog code written at the Behavioral level for a Design Unit.	4	2	5	1	1
16. a)	Mention the advantages of FPGA over ASIC in Digital System Design.	4	1	1	1	1
b)	Write a complete Verilog module 'bitmatch' with code at behavioral level, for comparing two 4-bit unsigned numbers a3a2a1a0 and b3b2b1b0 to produce an output y=1, if the two numbers match in at-least 3 bit positions.	4	3	2	2	1
17.	Answer any ***two*** of the following:					
a)	Design 4-bit Carry Look Ahead Adder using logic gates.	4	4	3	3	1
b)	Model a mod-100 Counter with Asynchronous active low reset, using Verilog HDL.	4	2	4	1	1
c)	Explain the role of FIFO in serial communication.	4	2	5	1	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	30%
iii)	Blooms Taxonomy Level – 3 & 4	50%

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